DATA SHEET

TDA8043
Satellite Demodulator and Decoder (SDD)

Preliminary specification
File under Integrated Circuits, IC02

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Satellite Demodulator and Decoder (SDD) TDA8043

FEATURES

- One chip Digital Video Broadcasting (DVB) compliant demodulator and concatenated Viterbi/Reed-Solomon decoder with de-interleaver and de-randomizer
- 3.3 V supply voltage (up to 5 V allowed)
- Internal clock divider
- On-chip crystal oscillator
- QPSK/BPSK demodulator:
  - Interpolator to handle variable symbol rates without an external anti-aliasing filter
  - On-chip Automatic Gain Control (AGC) of the analog input I and Q baseband signals or tuner AGC control
  - Two on-chip matched A/D converters (7 bits)
  - Square-Root Raised-Cosine Nyquist filter with programmable roll-off factor
  - High maximum symbol frequency: 32 Msymbols/s
  - Can be used at low channel Es/No (Symbol energy-to-noise ratio)
  - Internal carrier recovery, clock recovery and AGC loops with programmable loop filters
  - Two carrier recovery loops enabling phase tracking of the incoming symbols
  - Different modulation schemes: Quarter Phase Shift Keying (QPSK) and Bi-phase Shift Keying (BPSK)
  - Signal-to-noise ratio (S/R) estimation
  - External indication of demodulator lock
- Viterbi decoder:
  - Rate $\frac{1}{2}$ convolutional code based
  - Constraint length K = 7 with $G_1 = 171_{oct}$ and $G_2 = 133_{oct}$
  - Supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
  - 4 bit inputs for ‘soft decision’ for both I and Q
  - Truncation length: 144
  - Automatic synchronization
  - Channel BER (Bit Error Rate) estimation
  - External indication of Viterbi sync lock
  - Differential decoding supported
- Reed Solomon (RS) decoder:
  - (204, 188, T = 8) Reed Solomon code
  - Automatic (I^2C-bus configurable) synchronization of bytes, transport packets and frames
  - Internal convolutional de-interleaving (I = 12; using internal memory)
  - De-randomizer based on Pseudo Random Binary Sequence (PRBS)
  - External indication of RS decoder sync lock
  - External indication of uncorrectable errors (transport error indicator is set)
  - Indication of the number of lost blocks
  - Indication of the number of corrected blocks/bytes
- I^2C-bus interface:
  - I^2C-bus interface initializes and monitors the demodulator and Forward Error Correction (FEC) decoder with stand-by mode; when no I^2C-bus is used, default mode is defined
  - 4 bits I/O expander for flexible access to and from the I^2C-bus
- Package: PLCC84
- Boundary scan test.

APPLICATIONS

- Demodulation and error correction for digital satellite TV.

GENERAL DESCRIPTION

This document specifies a DVB compliant demodulator and error correction decoder IC for reception of QPSK and BPSK modulated signals for satellite applications.
The SDD (Satellite Demodulator and Decoder) can handle variable symbol rates without adapting the analog filters within the tuner. Typical applications for this device are:

- **Single-cast**: one QPSK/BPSK modulated signal in a single channel
- **Multi-cast**: two or more QPSK/BPSK modulated signals in a single channel
- **Simul-cast**: QPSK/BPSK modulated signal together with a Frequency Modulated (FM) signal in a single channel.

The SDD requires the two I and Q analog quadrature demodulated baseband signals as an input and provides 8-bit wide MPEG2 transport packet data at the output. The output of the SDD can be directly connected to the descrambler (SAA7206) or the demultiplexer (SAA7205).

The output can also be used to monitor internal data, for example I/Q after demodulation, data after Viterbi decoding and data after de-interleaving.

The SDD requires a single clock frequency which is independent to the received symbol rate as long as the clock frequency is slightly higher than twice the highest symbol frequency. This makes it possible to use a clock signal which already exists within the complete system.

All loops to recover the data from the received symbols are internal. No external loop components are required. Loop parameters for the clock and carrier recovery can be controlled by I^2C-bus.

The SDD can be controlled and monitored by I^2C-bus. An I^2C-bus default mode is specified which makes it possible to use the device with a minimum of software control. A 4-bit bidirectional I/O expander and an interrupt line is available. By sending an interrupt signal, the SDD can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS(1)	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	V_{DD} = 3.3 V; note 2	–	480	–	mA
f_{clk}	clock frequency		–	–	65	MHz
r_s	symbol rate		3	–	32	Msymbols/s
IL	implementation loss	note 2	–	0.3	–	dB
α	Nyquist roll-off (programmable)		–	35 or 50	50	%
P_{tot}	total power dissipation	T_{amb} = 70°C; note 2	–	1.5	tbf	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–	–	70	°C
T_j	operating junction temperature	T_{amb} = 70°C	–	–	125	°C
S/N	signal-to-noise ratio for locking the SDD (QPSK)		tbf	–	–	dB

Notes

1. This implementation was measured in a laboratory environment.
2. These values are specified for a symbol rate of 27.5 MSymbols/s.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8043K	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD1}	1	–	digital supply voltage 1
V_{SSD1}	2	–	digital ground 1
V_{AGC}	3	O	AGC output voltage
V_{DDD2}	4	–	digital supply voltage 2
V_{DDD3}	5	–	digital supply voltage 3
OUTSD	6	O	general purpose Sigma-Delta output
I0	7	I	digital bypass I-input ADC (bit 0)
I1	8	I	digital bypass I-input ADC (bit 1)
I2	9	I	digital bypass I-input ADC (bit 2)
I3	10	I	digital bypass I-input ADC (bit 3)
V_{SSD2}	11	–	digital ground 2
I4	12	I	digital bypass I-input ADC (bit 4)
I5	13	I	digital bypass I-input ADC (bit 5)
I6	14	I	digital bypass I-input ADC (bit 6)
Q0	15	I	digital bypass Q-input ADC (bit 0)
V_{DDD4}	16	–	digital supply voltage 4
Q1	17	I	digital bypass Q-input ADC (bit 1)
Q2	18	I	digital bypass Q-input ADC (bit 2)
Q3	19	I	digital bypass Q-input ADC (bit 3)
Q4	20	I	digital bypass Q-input ADC (bit 4)
V_{SSD3}	21	–	digital ground 3
Q5	22	I	digital bypass Q-input ADC (bit 5)
Q6	23	I	digital bypass Q-input ADC (bit 6)
V_{SSD4}	24	–	digital ground 4
V_{DDD5}	25	–	digital supply voltage 5
V_{DDD6}	26	–	digital supply voltage 6
PRESET	27	I	set device into default mode
P3	28	I/O	quasi-bidirectional I/O port (bit 3)
P2	29	I/O	quasi-bidirectional I/O port (bit 2)
P1	30	I/O	quasi-bidirectional I/O port (bit 1)
P0	31	I/O	quasi-bidirectional I/O port (bit 0)
V_{DDD7}	32	–	digital supply voltage 7
PKTBCLK	33	O	output clock for transport stream bytes (to SAA7205H)
PKTDAT0	34	O	parallel data output to SAA7205H (bit 0)
PKTDAT1	35	O	parallel data output SAA7205H (bit 1)
PKTDAT2	36	O	parallel data output SAA7205H (bit 2)
V_{SSD5}	37	–	digital ground 5
PKTDAT3	38	O	parallel data output SAA7205H (bit 3)
PKTDAT4	39	O	parallel data output SAA7205H (bit 4)
PKTDAT5	40	O	parallel data output SAA7205H (bit 5)

SYMBOL	PIN	I/O	DESCRIPTION
PKTDAT6	41	O	parallel data output SAA7205H (bit 6)
V_{DDD8}	42	–	digital supply voltage 8
V_{SSD6}	43	–	digital ground 6
V_{DDD9}	44	–	digital supply voltage 9
V_{DDD10}	45	–	digital supply voltage 10
PKTDAT7	46	O	parallel data output SAA7205H (bit 7)
PKTBAD	47	O	transport error indicator SAA7205H
PKTDATV	48	O	data valid indicator SAA7205H
PKTSYNC	49	O	transport packet synchronisation signal SAA7205H
V_{SSD7}	50	–	digital ground 7
SCL	51	I	serial clock of I^2C-bus
SDA	52	I/O	serial data of I^2C-bus
$\overline{INT}$	53	O	interrupt output (active LOW)
A0	54	I	I^2C hardware address
RSLOCK	55	O	Reed-Solomom lock indicator
VLOCK	56	O	Viterbi lock indicator
DLOCK	57	O	demodulator lock indicator
V_{DDD11}	58	–	digital supply voltage 11
TEST	59	I	test pin (normally connected to ground)
TRST	60	I	optional asynchronous resettlement (normally connected to ground)
TCK	61	I	dedicated test clock (normally connected to ground)
V_{DDD12}	62	–	digital supply voltage 12
V_{DDD13}	63	–	digital supply voltage 13
V_{SSD8}	64	–	digital ground 8
V_{SSD9}	65	–	digital ground 9
TMS	66	I	input control signal (normally connected to ground)
TDO	67	O	serial test data out
TDI	68	I	serial test data in (normally connected to ground)
V_{DDD14}	69	–	digital supply voltage 14
V_{SSD10}	70	–	digital ground 10
$V_{SSD(AD)}$	71	–	digital ground A/D converter
$V_{DDD(AD)}$	72	–	digital supply A/D converter
$V_{ref(N)}$	73	I	negative reference voltage for ADC
V_{SSA1}	74	–	analog ground 1
QA	75	I	analog input Q
$V_{ref(M)}$	76	I	mid-range reference voltage for ADC
IA	77	I	analog input I
V_{SSA2}	78	–	analog ground 2
I_{BIAS}	79	I	external reference current for ADC
V_{DDA}	80	–	analog supply voltage
V_{DDCL}	81	–	supply voltage for crystal oscillator

SYMBOL	PIN	I/O	DESCRIPTION
XTALI	82	I	clock oscillator input
XTALO	83	O	clock oscillator output
V_{DDXTAL}	84	–	supply voltage for crystal oscillator

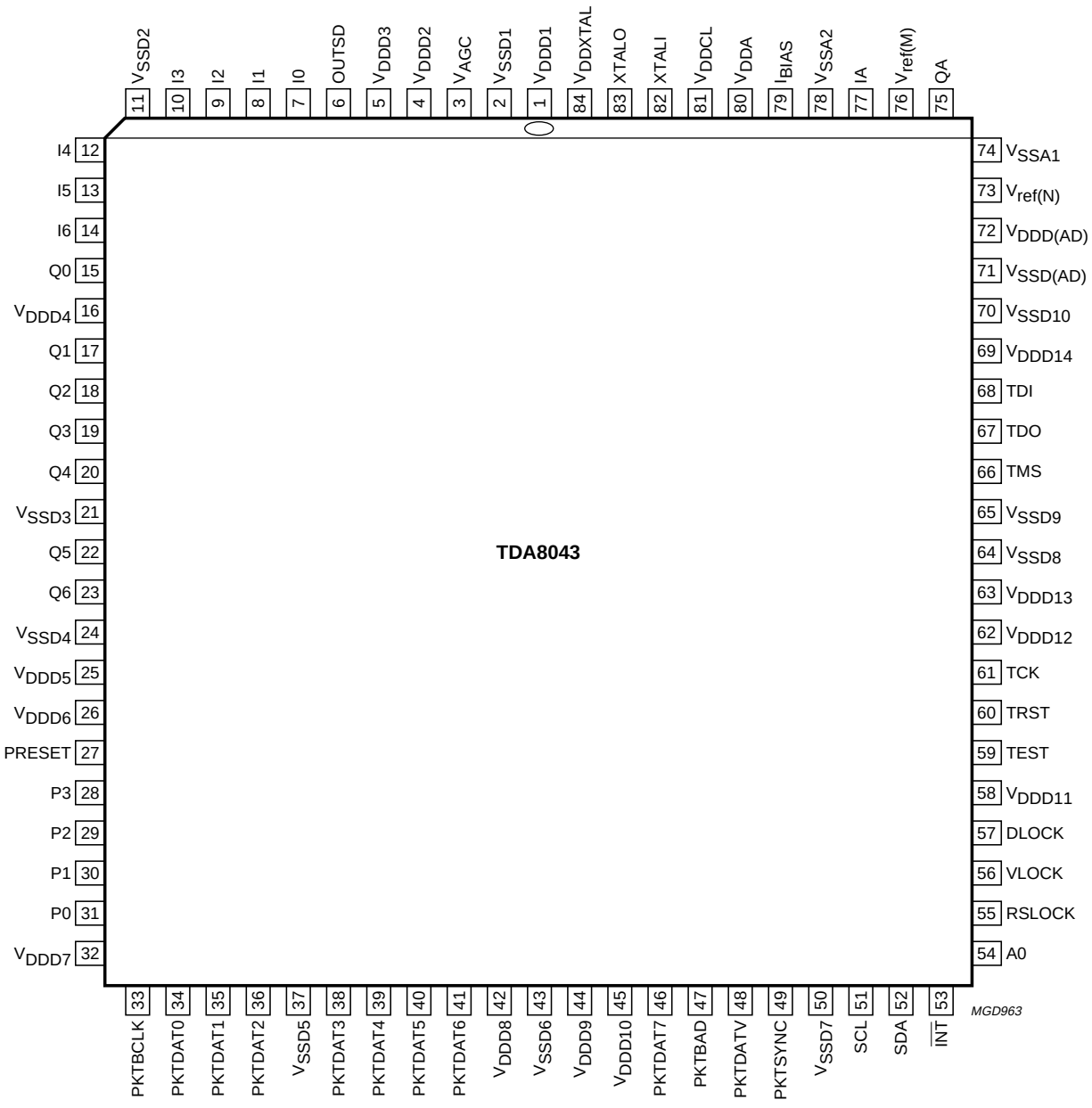
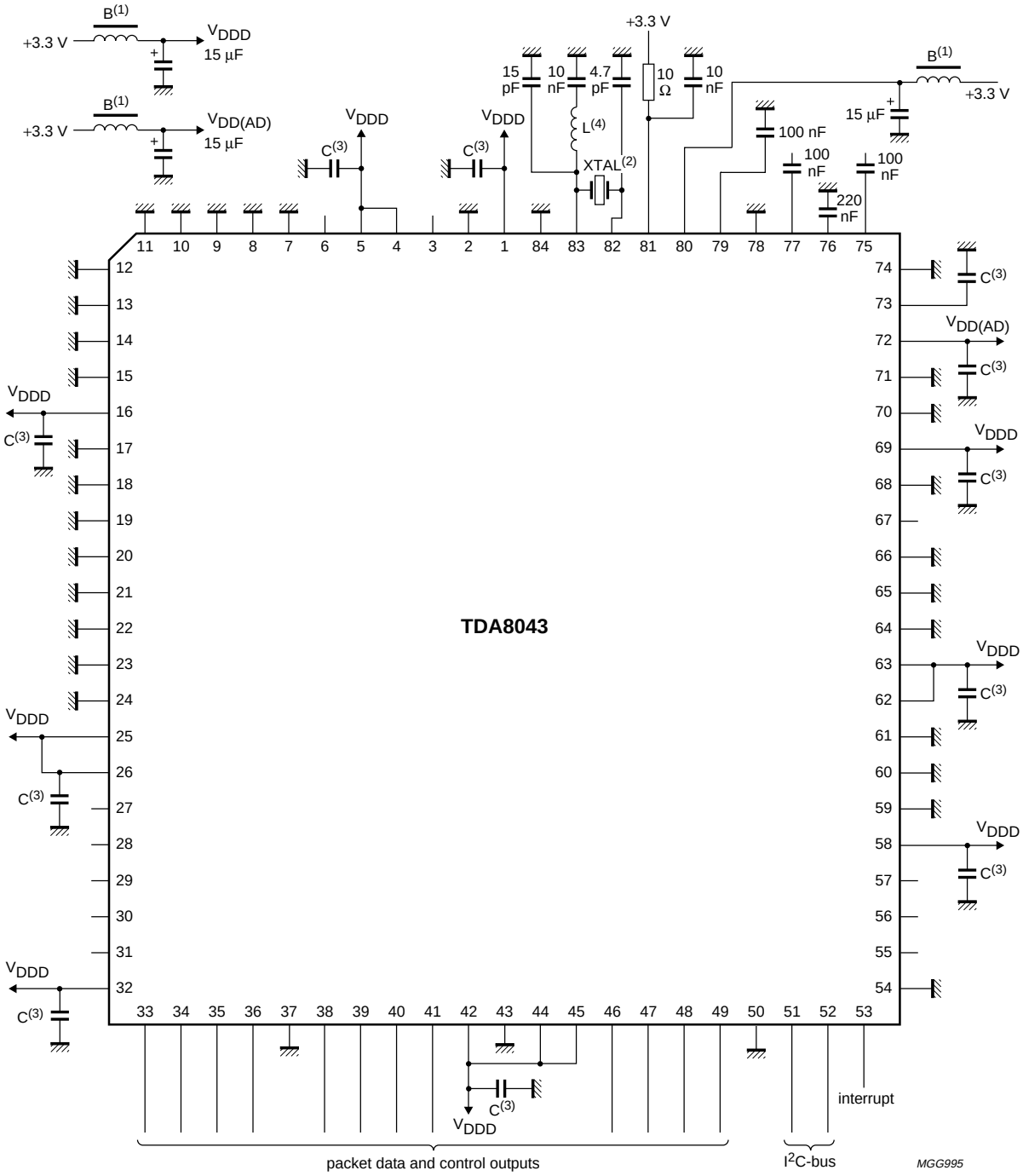


Fig.1 Pin configuration.

APPLICATION INFORMATION



(1) B = SMB bead type CBD8.9/3/3 Grade 4S2.
(2) X-tal = 65 MHz, 3rd harmonic.
(3) C = 6.8 nF, SMD.
(4) L = 560 nH, Talyo Yuden LAL02.

Fig.2 Application diagram

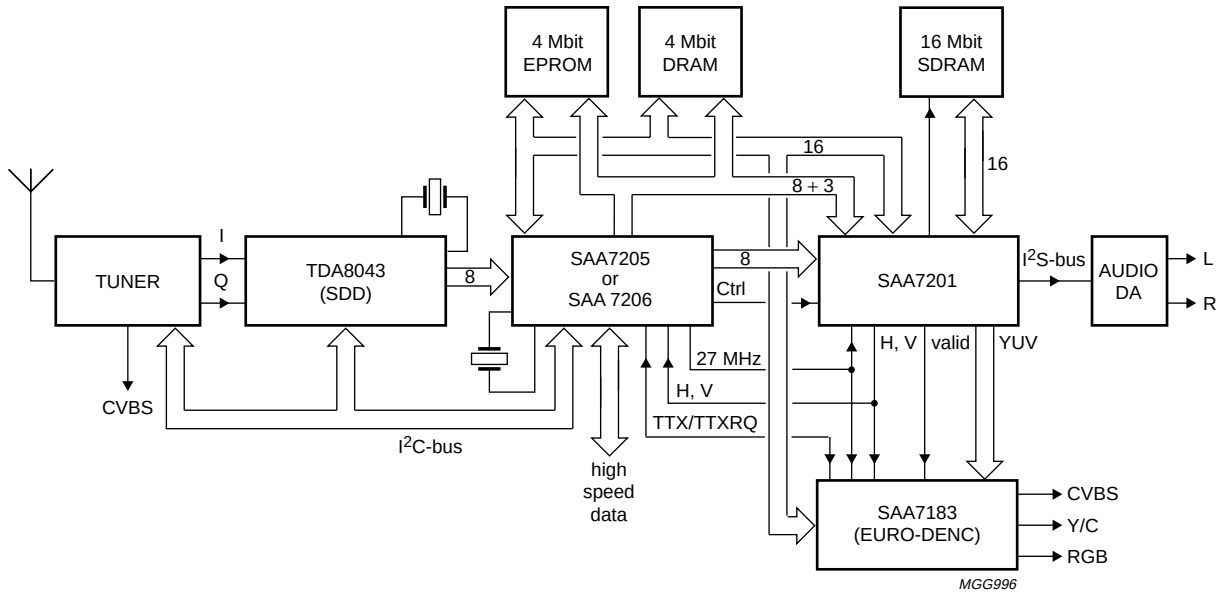
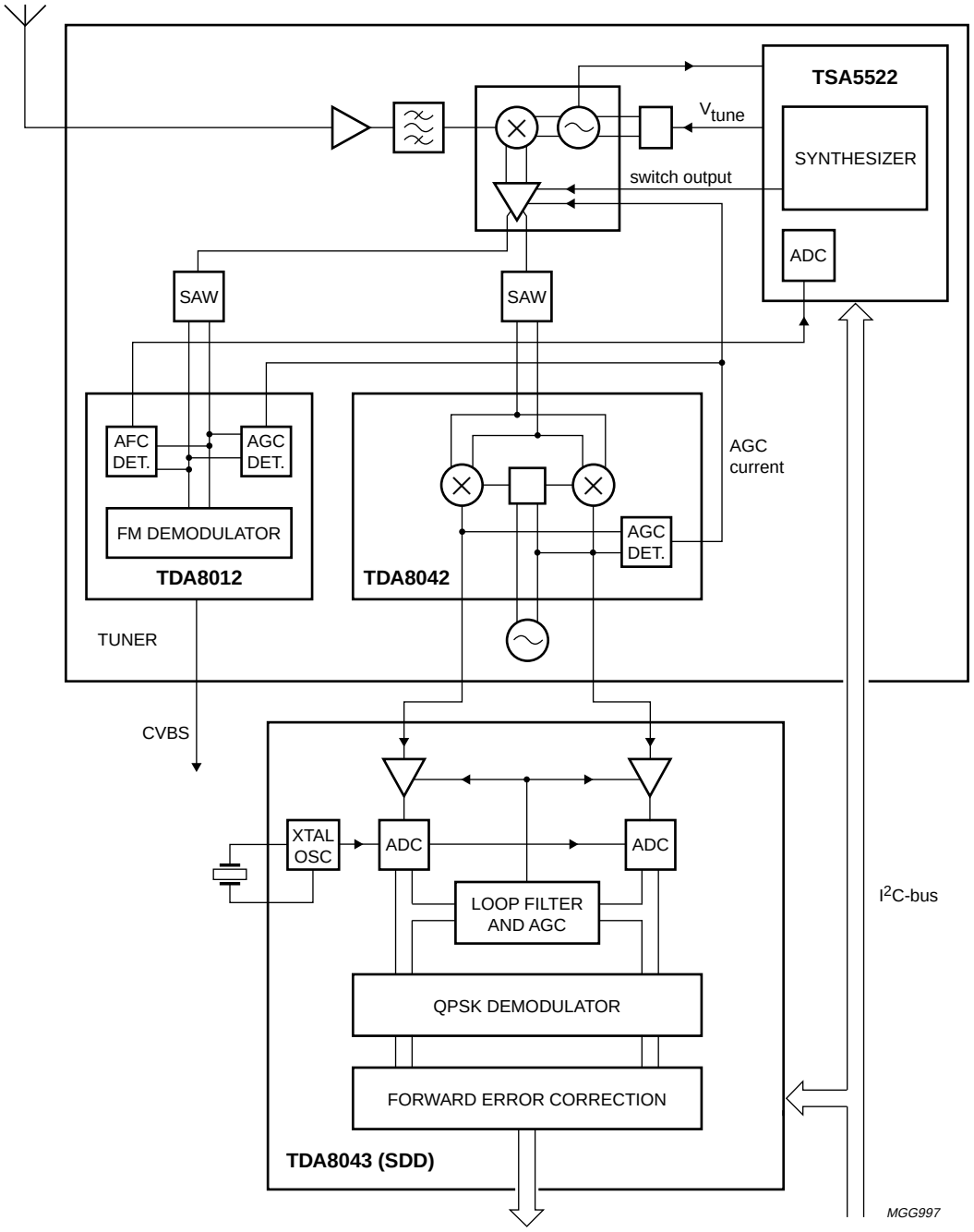


Fig.3 Satellite set-top decoder concept.

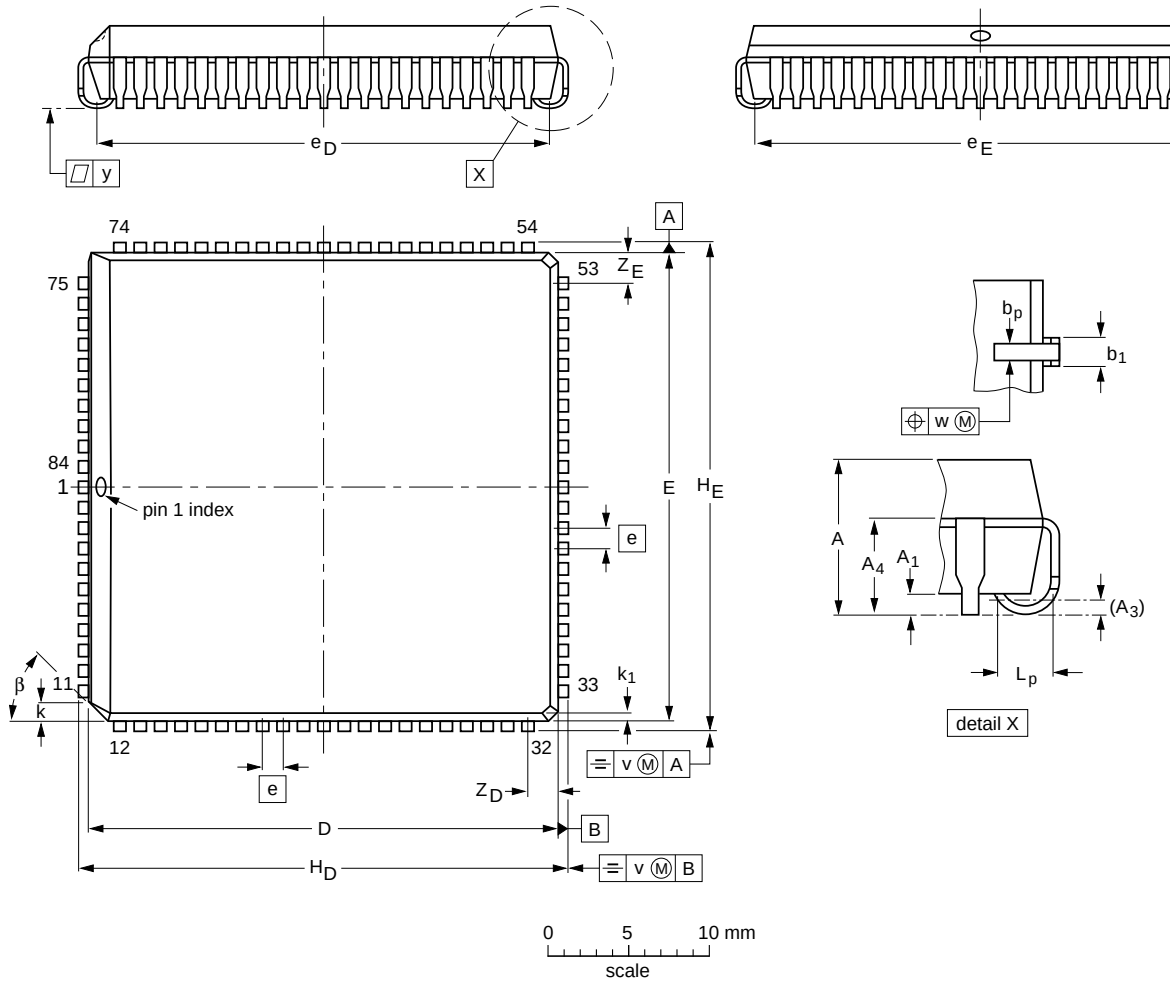


Control for external AGC is also available using the internal sigma-delta converter.

Fig.4 Application of satellite demodulator and decoder including tuner.

PACKAGE OUTLINE

PLCC84: plastic leaded chip carrier; 84 leads **SOT189-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45^o
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-2						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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